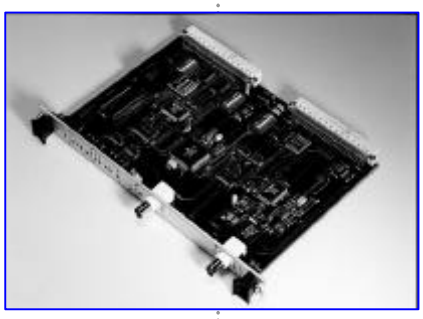
MICROSYSTEMES
Time-frequency & Networks

SR1623

VME Synchronization Board IRIG B time code reader & GPS receiver

Features

- Standard VME board. The board acquires the UT date & time either from an IRIG B source or a GPS receiver.
- The board is able to respond to many timing applications using the two available time sources and all the different means of generating timing signals
- The module is compatible with 16 or 32 bits VME bus. It needs a single 4 TE wide slot in the IRIG B only version or a double 8 TE wide slot in the version with a GPS receiver. The front panel provides many status leds, the input connectors for IRIG B and GPS Antenna.
- The IRIG B signal input uses an isolated BNC connector. The signal input is isolated by a transformer.
- The different 1 PPS signals : local, extracted from IRIG B, extracted from GPS receiver, are provided on a Sub'D test connector on the front panel. A green led "1 PPS" blinks at the biginning of every second..
- On the VME P2 connector, I/O are available for specific applications : RS232/RS422 outputs for sending time frames, TTL/RS422 outputs for timing signals (pulses or frequencies), TTL/RS422 inputs for precise external event time stamping.



INTERNAL TIME BASE

To keep the stability of the time in case of lacking of external synchronisation signals (IRIG B input or GPS 1PPS), the board has an internal 20 MHz VCXO oscillator with intrinsic stability of 2 10 –6 /year. When an synchronisation source is available, this oscillator will lock on it. All frequency and timing signal generated by the board a derived from this oscillator and remain all synchronised together.

DIALOG ON THE BUS

The dialog with the master processor on the bus uses a dual access memory in which the local processor writes the time and status information. In a symmetrical way, the bus master writes data and commands in this memory to configure and drive the board functions

READING THE TIME

The time can be read on the fly. The board freezes the data for the duration of the access of the whole time data to avoid time changes during an access.

PROGRAMMABLE I/O

The board generates four individually software programmable frequencies ranging from 1 Hz to 1 MHz. These frequencies can be routed to the TTL or RS422 outputs under software control.

PERIODIC INTERRUPTION

The board is able to send a periodic interrupt to the bus. The interrupt periodicity can be set by software. The range is 1 ms to 1 second with a 1 ms resolution. The interrupt level is set by a dip-switch. The interrupt vector is set by software.

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- To timestamp an event, the board is able to send a interrupt to the bus when an external strobe signal latches the current time. If this interrupt is active, all new events will be ignored until the interrupt request is served. The interrupt level is the same than for periodic interrupt. The interrupt vector is set by software and is specific for this interrupt. Even If the interruption is disabled, a bit is set in the status register to mention the occurrence of an event. All new events will be ignored until this flag is cleared by reading the event timestamp.

Specifications

- Resolution of the time : 1µs
- Precision of external event timestamp : 1 µs
- Programmable frequency generators : range 1 Hz to 1 MHz, 4 programmable divisors.
- Frequency outputs : TTL or differential RS422, 8 outputs, each can be connected to any of the 4 frequency generators.
- Maximum phase error between local 1 PPS and reference 1 PPS : < 10 µs (IRIG B), < 1 µs (GPS).
- Maximum phase error between frequency outputs (front edges) : < 50 ns.
- Serial time frame : RS232 or RS422 asynchronous serial link. Message syntax : YYYYQQQHHMMSS<CR><LF> (year, day number, hour, minute & second).
- Selection of reference source : software control.

Ordering information

SR1623-1 : Board without GPS receiver.

SR1623-2 : Board with GPS receiver.

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ZI du chapitre – 14, rue Jean Perrin
31100 Toulouse – France
Tél. : 33 - 5 62 87 10 70
Fax : 33 - 5 62 87 10 77
www.microsystemes.com