electronic consulting

Modelsim

vlog

Key Arguments (use- help for full list)

[-vlog95compat]	Disable Verilog 2001 keywords
[-compat]	Disable event order optimalization
[-f <filename>]	Pass in arguments from file
[-O5]	Maximum optimalization
[-hazards]	Enable run- time hazard cheking
[-help]	Display vlog syntax help
[-nodebug]	Hide internal variables & structure
[-quiet]	Disable loading messages
[-R <simargs>]	Invoke VSIM after compile
[-refresh]	Regenerate lib to current version
[-sv]	Enables SystemVerilog keywords
[-version]	Returns compiler version
[-v <library_file>]	Specify Verilog source library
[-work <libname>]	Specify work library
<filename(s)>	Verilog file(s) to be compiled

Examples

vlog top.v
vlog- work mylib- refresh

vcom

Key Arguments (use- help for full list)

[-2002] [-93] [-87]	Choose VHDL-02(default)-93-87
[-check_synthesis]	Turn on synthesis checker
[-debugVA]	Print VITAL opt status
[-O5]	Maximum optimalization
[-explicit]	Resolve ambiguous overloads
[-help]	Display **vcom** syntax help
[-f <filename>]	Pass in arguments from file
[-norangecheck]	Disable runtime range checking
[-nodebug]	Strip internal names
[-novitalcheck]	Disable VITAL95 checking
[-nowarn <#>]	Disable individual warning msg
[-O0]	Disable optimalization
[-quiet]	Disable loading messages
[-refresh]	Regenerate library image
[-version]	Returns compiler version
[-work <libname>]	Specify work library

Examples

vcom MyDesign.vhd
vcom -93- work/lib/mylib until.vhd
vcom -refresh

Code Coverage

Key Arguments to vcom/vlog

-cover bcesx	Specifies coverage type(s)

Key Arguments to vsim

-coverage	Enable statistics collection

sccom

Key Arguments (use- help for full list):

-link	Links source code, required
[CPP option]	C++ compiler option
[-g]	Compile with debugging info
[-nonamebind]	Disables automatic name binding
[-scv]	Includes SystemC verification libary
<filename(s)>	SystemC files to be compiled

Examples:

sccom- g example.ccp
sccom- link example
sccom- I/home/systemc/include- g a.cpp b.cpp

vsim

Key Arguments (use- help for full list)

[-c]	Run in cmd line mode
[-coverage]	Invoke Code Coverage
[-do "cmd" | <file>]	Run cmd or file at startup
[-elab]	Create elaboration file
[-f <filename>]	Pass in args from file
[-gIG<name=value>]	Set VHDL Generic values
[-hazards]	Enable hazard checking
[-help]	Display vsim syntax help
[-l <logfile>]	Save transcript to log file
[-load_elab]	Simulate an elaboration file
[+notimingchecks]	Disable timing checks
[-quiet]	Disable loading messages
[-restore <filename>]	Restore a simulation
[-sdf{minltyplmax}	Apply SDF timing data i.e.
<region>=<sdffile>]	-sdfmin /top=MySDF.txt
[-sdfnowarn]	Disable SDF warnings
[-t [<mult>]<unit>]	Specify time resolution
[-version]	Returns vsim version
[-view <filename>]	Log file for VSIM to view
[-wlf <filename>]	Log file to create
[<libname>.<design_unit>]	Configuration, Module,

Examples:

vsim top
vsim -lib mywork top -do commands.do

modelsim.ini

Copy modelsim.ini to current directory

Execute **vmap -c**

Loading order (stops after finding first file)

1. $MODELSIM environment variable
2. Current directory if $MODELSIM is not set
3. In /<install_dir>/modeltech/<platform> dir
4. In /<install_dir>/modeltech directory

For Detailed Information see:

ModelSim Ref Man "System Initialization/ProjectFile"

modelsim.tcl

Loading order

Always loads: /<install_dir>/modeltech/tcl/vsim/pref.tcl
Loads the first found from:
1. $MODELSIM_TCL if it exists (":" separated list)
(all files in list are loaded)
2. Current directory ./modelsim.tcl
3. $HOME/modelsim.tcl

Environment Variables (see ModelSim cmd "**printenv**")

LM_LICENSE_FILE	**Required**	Pathname of license.dat file

DOPATH	Optional	Search path for ".do" files
EDITOR	Optional	Specifies editor for "edit" cmd
MODELSIM	Optional	Pathname of modelsim.ini file
MODELSIM_TCL	Optional	List of modesim.tcl libraries
MODEL_TECH_TCL	Optional	Pathname to Tcl/Tk libraries

MODEL_TECH	**Don't Set**	Used internally by ModelSim
MGC_LOCATION_MAP	Optional	Used as "soft" path to find files
PLIOBJS	Optional	Used to load PLI object files
TMPDIR	Optional	Used by VSIM for temp space

Language Syntax

command arg1 arg2 arg3 ...

Language Syntax: Command

set <var> <value>
expr <math expression>
exec <ShellCommand>
info <option> <procedure name>
winfo <option> <window name>

Language Syntax: Procedures

proc name {arglist} {body}
proc dag {a b} {
Set c [expr sqrt($a*$a + $b
Return $c}

Language Syntax: Conditionals

if {boolean} {bodytrue} else {bodyfalse}
If {$now < 10000} {echo $now}

Language Syntax: Loops

while {boolean} {body}
foreach loopVar {valuelist} {cmdBody}
for {initial} {test} {final} {body}

Poking around in ModelSim Tcl/Tk

info	Get into on a Tcl construct
info xx	Find out the args to info
winfo	Get info on Tk widgets
winfo xx	Find out args to winfo
winfo children	Return sub- widgets to ModelSim
lecho [configure wave]	Get wave props

Wave Window

add wave <item>	Wave specific signals/nets
add wave *	Wave signals/nets in scope
add wave -r /*	Wave all signals/nets in design
add wave abus(31:15)	Wave a slice of a bus
view wave	Display wave window
view wave -new	Display additional wave window
write wave	Print wave window to file
<left mouse button>	Select signal / Place cursor
<middle mouse button>	Zoom options
<right mouse button>	Zoom Popup Menu
<ctrl-f>	Find next item
<tab> (go right)	Search forward for next edge
<shift-tab> (go left)	search backward for next edge
I i or + | o O or -	Zoom in | Zoom out
f or F | l or L	Zoom full | Zoom Last

Key ModelSim Commands

Commands may be used in the following locations: (Sh)ell, (M)odelSim> prompt, or (V)SIM> prompt. See Command Reference for complete command list and syntax.

vcom	Sh, M, V	VHDL Compiler)
vdel	Sh, M, V	Delete a design unit from a specific library
vdir	Sh, M, V	Lists the contents of a library
vlib	Sh, M, V	Creates a design library
vlog	Sh, M, V	Verilog Compiler
sccom	Sh, M, V	SystemC Compiler
vmap	Sh, M, V	Defines or displays library mappings
vopt	Sh, M, V	Optimize design
vsim	Sh, M, V	VHDL and/or Verilog Simulator
add list | wave	V	Add signals to the List or Wave windows
add log	V	Log signals to vsim.wlf file for analysis later
alias	M,V	Create a user defined alias (e.g., alias h "history")
bp,bd	V	Set/Clear a breakpoint
cd	Sh,M,V	Change directory
change	V	Modify a VHDL variable or Verilog register
checkpoint	V	Save the state of you simulation (see restore)
compare add	M,V	Compare signals
configure	M,V	Configure List or Wave window attributes
delete	V	Remove HDLitem from List or Wave window
do	M,V	Execute a file of commands (e.g., do macro.do)
drivers	V	Display current and future value of signal or net drivers
dumplog64	Sh	Dump the contents of the vsim. Wlf file in a redable form
echo	M,V	Display message (e.g., echo "Time is $now ns.")
edit	M,V	Invoke editor specified by the EDITOR env variable
environment	M,V	Display or change current region/signal environment
examine	M,V	Examine one or more HDL items (e.g., exa /top/clk)
find	V	Display pathnames of matching HDL items
force	V	Force signals or nets (e.g., force clk 1 10, 0 20 -r 100)
history	M,V	List previous commands
noforce	V	Release signals or nets from force commands
notepad	M,V	Simple text editor
printenv	M,V	Display names and values of environment variables
profile on	M,V	Turn on Performance Analyzer
property	V	Change List or Wave signal attributes (color, radix, etc.)
pwd	M,V	Display current path in Main transcript window
radix	M,V	Change the default radix in all windows
report	M,V	returns all control or state variable values
restart	V	Restart the simulator
restore	M,V	Restore the simulation state from a previous checkpoint
resum	M,V	Resume macro execution after a pause command
right 7 left	V	Search in wave window for next transition or -expr
run	V	Advance simulation time (e.g, run 1000)
rearch / next	V	Search specified window for next item matching pattern
seetime	V	Scroll List or Wave window to time (e.g., seetime wave 500)
vdc2wlf	Sh	Translate VCD file into WFL file
vcddumpports	M,V	Create a VCD file
vcover merge	Sh, M, V	Merges coverage reports
vgencomp	Sh	Create VHDL component from complied Verilog module
view	M,V	Open a ModelSim window and pop it to the top
vmake	Sh	Print a makefile for a library
vsource	V	Display HDL source file in Source window
when	M,V	Perform action on condition (e.g., when clk=1 {echo clk}
where	M,V	Display info about the environment
write	M,V	Records names, window contents, and preferences to a file Repeat
!! | !n	M,V	Repeat last command, Repeat nth command
!abc	M,V	Repeat cmd starting "abc"
^abc^xyz	M,V	Replace "abc" in previous command with "xyz"

Files

modelsim.ini

Simulator Initialization file; stores library locations, simulator resolution, paths, etc.

modelsim.tcl

Window sizes, positions,colors, etc. User Tcl/Tk code

startup.do

Default name of macro executed after design is loaded; See “startup=” line in modelsim.ini

transcript

Default filename that ModelSim transcript window activity is saved to vsim.wlf Default name of simulation log file saved by VSIM

Managing Breakpoints

bp	Sets a breakpoint; without arg shows all bps
bd	Deletes a breakpoint
Disablebp	Turn off all breakpoints
enablebp	Turns all breakpoints on
onbreak	Define what to do when a breakpoint is hit during a macro (e.g., **onbreak** {**resume**})
when	Perform actions under certain conditions

Performance

Key arguments to vopt

-o <name>	Optimized design name
<design>	Top-level design unit
[+acc=[<spec>]+ [<module>]]	Enable design object visibility

Key arguments to vsim

[-elab]	Create elaboration file
[-load_elab]	Simulate elaboration file

Signal Spy

init_signal_driver	Drive hierarchical signal
init_signal_spy	Read hierarchical signal
signal_force	Force hierarchical signal
signal_release	Release hierarchical signal

PSL

Key arguments to vcom and vlog

[-pslfile <file>	External PSL file

Key Commands

assertion fail	Assertion failure response
assertion pass	Assertion pass response
assertion report	Assertion status report
fcover clear	Clear coverage meta-data
fcover clear	Adds meta-data to coverage database
fcover configure	Functional coverage target configuration
fcover report	Functional coverage results report
fcover save	Save data to reloadable file
fcover vcover merge	Merge coverage data files offline